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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,323	09/14/2000	Seiichi Matsui	0879-0277P	1512

2292 7590 08/25/2005

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EXAMINER	
JERABEK, KELLY L	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,323	MATSUI, SEIICHI	
	Examiner	Art Unit	
	Kelly L. Jerabek	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-12 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-12 and 16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 7/10/2005 have been fully considered but they are not persuasive.

Response to Remarks:

Applicant's arguments (Amendment page 11) state that in contrast to the Harada reference the present invention as set forth in claim 4 discloses an imaging apparatus comprising a timing generator that drives the solid imaging device and reads pixel information from the solid imaging device, the timing generator applying gate pulses for transferring only pixel information of pairs of two adjoining lines with intervals of a plurality of lines to vertical transferring routes to the transferring gates when image signals with low definition are produced. Applicant's arguments further state that the interlacing described in Harada et al. is not from "each pair of two adjoining lines read from solid imaging device when image signals with low definition are produced". The Examiner agrees that the Harada reference does not teach a timing generator for applying gate pulses for transferring only pixel information of pairs of two adjoining lines with intervals of a plurality of lines to vertical transferring routes to the transferring gates when image signals with low definition are produced. However, the Yamaguchi

reference discloses this feature. The Harada reference is cited for the purpose of disclosing a method of producing pixel information of one line from pixel information of two adjoining lines. Therefore, the 103 rejection combining the Yamaguchi and Harada references discloses all of the limitations of claims 4-7, 9-12, 16-19, and 21-24 (See 103 rejection from previous action).

Applicant's arguments (Amendment page 12) state that one skilled in the art would not have been motivated to combine the Yamaguchi and Harada references because the mode described by Yamaguchi is low resolution while the mode in Harada is high resolution. The Examiner respectfully disagrees. **Although the Yamaguchi reference discloses a thinning operation for readout and the Harada reference discloses a method where all of the pixels of an imaging array are read out, this does not prevent the two references from being combined. The Harada reference is cited for the purpose of disclosing a method of producing pixel information of one line from pixel information of two adjoining lines (interlacing) and the Yamaguchi reference discloses applying gate pulses for transferring only pixel information of pairs of two adjoining lines with intervals of a plurality of lines.** Therefore, the 103 rejection combining the Yamaguchi and Harada references discloses all of the limitations of claims 4-7, 9-12, 16-19, and 21-24. The Examiner is rejecting the claims using the following 103 combination of the references:

Yamaguchi discloses in figure 14 an image pickup device capable of both full frame operation and line thinning operation. It can be seen in figure 15A that pixel information of two adjoining lines of the array composes color information of three primary colors (R,G,B) (col. 13, lines 30-32). The image pickup device includes photosensors (2) for acquiring image signals and vertical transferring routes (3) for reading out image signals (col. 13, lines 32-44). The vertical transferring routes (3) include a matrix of transferring gates (21,22,23,31,32,33) associated with the individual photosensors (2) (col. 13, lines 44-52). Driving pulses (φ V1, φ V2, φ V2', φ V3) are applied to the gates (21,22,23,31,32,33) via bus wirings (41,42,42',43) in order to transfer signals from the photosensors (2) according to either a full-frame operation or a line thinning operation (col. 13, line 48 – col. 15, line 4). During the line thinning operation only pixel information of certain photosensors (2) is readout and thus image signals with low definition are produced (fig. 16C; col. 14, line 46 – col. 15, line 4). The line thinning mode may be set so that only pixel information of pairs of two adjoining lines with intervals of a plurality of lines are transferred to the vertical transferring routes (3) thus reducing the number of output lines to half of the value (fig. 19, col. 16, lines 8-14). Additionally, Yamaguchi discloses a lens system (100) that forms a subject image on the CCD (101) (col. 5, lines 28-43). The image pickup device disclosed by Yamaguchi also includes a timing controller (107) for generating driving pulses for transferring pixel information according to the functions described above. However, Yamaguchi does not disclose a signal processing device that produces pixel information

of one line from the pixel information of each pair of two adjoining lines when image signals of low definition are produced.

Harada discloses in figure 1 an imaging apparatus (1) including a solid imaging device (14-16) and an optical system (3). The imaging apparatus (1) disclosed by Harada includes a signal processing device (72) that produces image signals by producing pixel information of one line from the pixel information of a pair of two adjoining lines read from the solid imaging device (fig. 9; col. 34, lines 23-41). Therefore, it would have been obvious for one skilled in the art to have been motivated to include the signal processing device capable of producing image signals by producing pixel information of lone line from the pixel information of a pair of adjoining lines as disclosed by Harada in the image pickup device capable of performing a line thinning operation as disclosed by Yamaguchi. **Doing so would provide a means for adding signals outputted from two adjacent light-receiving regions to generate a single output in each field (Harada: col. 34, lines 20-27).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7, 9-12, 16-19, and 21-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Harada et al. US 6,108,036.

Re claim 4, Yamaguchi discloses in figure 14 an image pickup device capable of both full frame operation and line thinning operation. It can be seen in figure 15A that pixel information of two adjoining lines of the array composes color information of three primary colors (R,G,B) (col. 13, lines 30-32). The image pickup device includes photosensors (2) for acquiring image signals and vertical transferring routes (3) for reading out image signals (col. 13, lines 32-44). The vertical transferring routes (3) include a matrix of transferring gates (21,22,23,31,32,33) associated with the individual photosensors (2) (col. 13, lines 44-52). Driving pulses (φ V1, φ V2, φ V2', φ V3) are applied to the gates (21,22,23,31,32,33) via bus wirings (41,42,42',43) in order to transfer signals from the photosensors (2) according to either a full-frame operation or a line thinning operation (col. 13, line 48 – col. 15, line 4). During the line thinning operation only pixel information of certain photosensors (2) is readout and thus image signals with low definition are produced (fig. 16C; col. 14, line 46 – col. 15, line 4). The line thinning mode may be set so that only pixel information of pairs of two adjoining lines with intervals of a plurality of lines are transferred to the vertical transferring routes (3) thus reducing the number of output lines to half of the value (fig. 19, col. 16, lines 8-14). Additionally, Yamaguchi discloses a lens system (100) that forms a subject image on the CCD (101) (col. 5, lines 28-43). The image pickup device disclosed by

Yamaguchi also includes a timing controller (107) for generating driving pulses for transferring pixel information according to the functions described above. However, Yamaguchi does not disclose a signal processing device that produces pixel information of one line from the pixel information of each pair of two adjoining lines when image signals of low definition are produced.

Harada discloses in figure 1 an imaging apparatus (1) including a solid imaging device (14-16) and an optical system (3). The imaging apparatus (1) disclosed by Harada includes a signal processing device (72) that produces image signals by producing pixel information of one line from the pixel information of a pair of two adjoining lines read from the solid imaging device (fig. 9; col. 34, lines 23-41). Therefore, it would have been obvious for one skilled in the art to have been motivated to include the signal processing device capable of producing image signals by producing pixel information of lone line from the pixel information of a pair of adjoining lines as disclosed by Harada in the image pickup device capable of performing a line thinning operation as disclosed by Yamaguchi. Doing so would provide a means for adding signals outputted from two adjacent light-receiving regions to generate a single output in each field (Harada: col. 34, lines 20-27).

Re claim 5, Yamaguchi states that the image pickup device may operate in a full-frame mode to readout signals of all pixels from the photosensors (2) to the vertical transferring routes (3) (col. 14, lines 8-16).

Re claim 6, when the image pickup device operates in full-frame mode the signals are divided into a plurality of fields (R,G,B) corresponding to the order of the array of color filters (col. 14, lines 8-16).

Re claim 7, the signal processing device (72) disclosed by Harada reduces pixel information of horizontal lines by producing pixel information of one line from the pixel information of pairs of adjoining lines by a process called interlacing (col. 34, lines 23-42; fig. 9).

Re claim 9, the image pickup device disclosed by Yamaguchi includes a liquid crystal display (135) for displaying color images read out according to either the full frame mode or the line-thinning mode (col. 8, lines 57-67).

Re claim 10, the image pickup device disclosed by Yamaguchi includes memory (143) that records the image signals produced by the image pickup device (col. 8, line 57 – col. 9, line 6).

Re claim 11, see claim 5.

Re claim 12, see claim 6.

Re claim 16, see claim 4.

Re claim 17, see claim 5.

Re claim 18, see claim 6.

Re claim 19, see claim 7.

Re claim 21, see claim 9.

Re claim 22, see claim 10.

Re claim 23, see claim 5.

Re claim 24, see claim 6.

Claims 8 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Harada et al. and further in view of Dischert US 6,040,869.

Re claim 8, Yamaguchi in view of Harada discloses all of the limitations according to claim 4. In addition, the signal processing device (72) disclosed by Harada

outputs the interlaced signals (col. 34, lines 20-23). However, Harada does not state that the signal processing device (72) has an interpolation operation device that interpolates the interlaced signals.

Dischert discloses in figure 1A video signal processing circuitry. The circuitry serves to interpolate interlaced lines (fig. 2D; col. 5, lines 57-65). Therefore, it would have been obvious to include the video signal processing circuitry as disclosed by Dischert in the solid imaging device disclosed by Yamaguchi in view of Harada. Doing so would provide a means for interpolating the interlaced signals with the low definition to produce modified image signals (Dischert: col. 5, lines 57-65).

Re claim 20, see claim 8.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran can be reached at **(571) 272-~~7564~~ 7382**. The fax phone number for submitting all Official communications is **(571) 273-8300**. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLJ

THAI TRAN
PRIMARY EXAMINER